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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,763	03/20/2001	Ossi Ilari Grohn	1280.00282	8886

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/812,763	GROHN, OSSI ILARI	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-15* is/are allowed.

6)☒ Claim(s) *20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 05/23/2005. Claims 1-15 and 20-23 are pending in this Office action.

Response to Arguments

2. Applicant's arguments, see page 7, filed on 05/23/2005, with respect to the rejection(s)of claim(s) 16-19 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn after Applicant cancelled claims 16-19. However, upon further consideration, a new ground(s) of rejection is made in view of Pearce U.S. Patent 5,515,404.

Claim Objections

3. Applicant is advised that should claim 21 be found allowable, claim 22 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pearce U.S. Patent 5,515,404.

Regarding claim 16, Pearce discloses a jitter-generating device for *use in data communication system*. The device shown in figure 2 includes a clock phase (jitter) modulation generator 13 for generating a controlled jitter. The clock phase modulator connected to the input of a phase locked loop (clock signal generator) 14 for modulating the phase of the clock signal output by the PLL 14. In column 3 lines 25-45, Pearce further teaches that the amplitude and frequency of the jitter generated by the modulation generator 13 is controlled by a jitter control system 17 via input 16.

Pearce does not teaches "providing a data signal having an encoded format of binary ones and zeros such that the appearance of a binary one in the data signal causes the phase modulation of the clock pulse signal by the selection of one of the jitter frequencies of a given amplitude, and the appearance of a binary zero causes selection of another frequency of given amplitude to thereby modulate the clock pulse signal to provide a phase modulated clock pulse signal that includes the encoded data".

In column 4, lines 2-15, in some cases, the adder 12 only passes on the output of the modulation generator 13 to the output PLL 14. In this case any jitter in the input signal is absorbed within the FIFO buffer 11, and the jitter in the output data is entirely that introduced by the modulation generator 13. In view of that, by keeping the amplitude constant and varying the frequency of the jitter, it would have been obvious for one of ordinary skill in the art at the time of the invention that Pearce teachings can be modified in such a way that for binary input, all 1's causes the phase modulation of the clock pulse signal by the selection of one of the jitter frequencies of a given amplitude, and the appearance of a binary zero causes selection of another frequency of given amplitude to thereby modulate the clock pulse signal to provide a phase modulated clock pulse signal that includes the encoded data as claimed in the application claim. Motivation is that in column 2, lines 1-15, Pearce teachings develops a jitter generating device that can be used to act as a repeater in a conventional data communication system. Therefore, the act of varying jitter frequencies cause frequency modulation on data sequence.

Regarding claims 21-22, as recited in claim 20, the amplitude and frequency of the jitter generated by the modulator generator 13 is controlled by a jitter control system 17 via an input 16. And the phase modulation can take a form of a sinewave of adjustable depth and frequency; see column 3, lines 50-65. In light of that, one of ordinary skill in the art at the time the invention was made would have recognized that

the jitter introduced could be implemented in three ways: having different frequencies and different amplitudes, having same frequencies and different amplitudes, having different frequencies and same amplitudes. The claimed limitations are within the scope of Pearce teachings.

Allowable Subject Matter

5. Claims 1-5 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 1, claim 1 is allowed over prior art of record since the cited reference (US 5,515,404 and US 6,076,175) taken individually or in combination fails to particularly disclose an enhanced capacity communication system comprising uniquely distinct features "*a phase modulator that receives an additional data signal and the transmit clock pulse signal, the phase modulator provides a sinusoidal jitter modulation that phase modulates the clock pulse signal by introducing intentional jitter at clock pulse transitions responsive to the additional data signal, the additional data signal thereby modulates the transmit clock pulse signal to provide a phase modulated transmit clock pulse signal that is delivered to the framer for inclusion with the data signal to create a combined data signal and additional data signal that is transmitted via the communication link to the receiving device for decoding and further use*".

6. Claims 6-11 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 6, claim 6 is allowed over prior art of record since the cited reference (US 5,515,404 and US 6,076,175) taken individually or in combination fails to particularly disclose an enhanced capacity communication system comprising uniquely distinct features "*a phase modulator that receives an additional data signal and the transmit clock pulse signal, the phase modulator provides a sinusoidal jitter modulation that phase modulates the clock pulse signal by introducing intentional jitter at clock pulse transitions, the sinusoidal jitter modulation having selectable jitter frequencies each having a given amplitude, the additional data signal having additional data encoded in a format of binary ones and zeros, such that the appearance of binary one in the additional data signal causes the phase modulator to select one of the jitter frequencies of a given amplitude, whereas the appearance of binary zero causes the phase modulator to select another frequency of a given amplitude, the additional data signal thereby modulates the transmit clock pulse signal to provide a phase modulated transmit clock pulse signal that is delivered to the framer for inclusion with the data signal to create a combined data signal and additional data signal that is transmitted via the communication link to the receiving device for decoding and further use*".

7. Claims 12-15 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 12, claim 12 is allowed over prior art of record since the cited reference (US 5,515,404 and US 6,076,175) taken individually or in combination fails to particularly disclose an enhanced capacity communication system comprising uniquely distinct features "*the data encoded signal having encoded format of binary ones and zeros, such that the appearance of binary one in the data encoded signal causes the phase modulation of the clock pulse signal by the selection of one of the jitter frequencies of a given amplitude, and the appearance of binary zero causes selection of another frequency of a given amplitude to thereby modulate the clock pulse signal and provide the phase modulated clock pulse signal that includes the data on the data encoded signal*".

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mesuda et al. U.S. Patent 5,598,130 discloses "Phase Modulator Capable Of Individually Defining Modulation Degree And Modulation Frequency".

Kobayashi U.S. Patent 6,493,408 B1 discloses "Low-Jitter Data Transmission Apparatus".

Flugstad et al. U.S. Patent 4,810,937 discloses "Frequency Modulation In Phase-Locked Loops".

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh cong Tran 08/05/2005

KCT

Examiner KHANH TRAN